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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/570,150	10/30/2006	Freddy Petersen	ALB.023	8038

20987 7590 02/25/2009

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EXAMINER	
NGUYEN, HOAI AN D	
ART UNIT	PAPER NUMBER
2831	

MAIL DATE	DELIVERY MODE
02/25/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/570,150	PETERSEN ET AL.	
	Examiner	Art Unit	
	HOAI-AN D. NGUYEN	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11 and 13-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 21-28* is/are allowed.

6)☒ Claim(s) *11,13,14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of the Amendment filed on January 30, 2009. Claim 12 is cancelled; claims 11, 13-20 and newly submitted claims 21-28 are pending in the application.

Specification

2. The disclosure is objected to because of the following informalities: the sub-heading "BRIEF" on page 1, line 27 should be replaced with -- BRIEF SUMMARY OF THE INVENTION --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 11, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kasdan et al.

Kasdan et al. teaches a diffraction pattern amplitude analysis for use in fabric inspection comprising:

With regard to claim 11, a pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1) for determination of the pulse height distribution of electronic pulses,

comprising a set of comparators (FIG. 6 in view of FIG. 2, a series of individual comparators 56) provided with a common input (FIG. 6, common video signal) for analog to digital conversion of the electronic pulses into converted pulses, a set of latches (FIG. 6 in view of FIG. 2, a series of latches 57) wherein inputs of the latches are connected to outputs of respective comparators for recording passage of corresponding threshold voltages by rising edges of the converted pulses, a priority encoder (FIG. 6, enabling circuits 64) connected to outputs of the latches for determination of pulse height categories (FIG. 6, Bin 0, Bin 1, Bin 2, Bin 3, Bin 4, Bin 5, Bin 6 and Bin 7) consisting of converted pulses with a pulse height within pulse height intervals defined by the corresponding threshold voltages ((0v, 1.25v) for Bin 0, ((1.25v, 2.5v) for Bin 1, and so forth for bin 2, bin 3, bin 4, bin 5, bin 6 and finally bin 7, wherein the reference voltages progressively increase in steps of 1.25 volts), and a micro controller (FIGS. 1, 2 and 6, processor 19 includes a series of counters 58) that is adapted to count a number of pulses within each pulse of the height categories (From column 7, line 52 to column 8, line 27).

In addition, claim 11 is directed to an apparatus whose feature is further recited functionally ("wherein the threshold voltages of the comparators are non-equidistant from each other"). However, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function alone (See MPEP 2114). The comparators (FIG. 6 in view of FIG. 2, a series of individual comparators 56) are configured such that the threshold voltages progressively increase in steps of 1.25 volts as disclosed in column 8, lines 38-44. Therefore, these comparators are fully capable of being configured such that the threshold voltages of the comparators are non-equidistant from each other as recited in claim 11.

With regard to claim 16, a plurality of sets of comparators (FIG. 6 in view of FIG. 2, a series of individual comparators 56) for pulse height determination of input electronic pulses of different amplification (FIG. 4, V_0, V_1, V_2, and so on).

With regard to claim 17, circuitry (FIG. 6 in view of FIG. 2, fixed frequency clock pulse generator 23) for resetting the latches (FIG. 6 in view of FIG. 2, a series of latches 57) a predetermined time period after start of a converted pulse, the time period being independent of the pulse height and pulse width (Column 8, lines 1-15).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Flockencier (US 5,357,331 A).

Kasdan et al. teaches a diffraction pattern amplitude analysis for use in fabric inspection comprising:

With regard to claim 11, a pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1) for determination of the pulse height distribution of electronic pulses, comprising a set of comparators (FIG. 6 in view of FIG. 2, a series of individual comparators 56) provided with a common input (FIG. 6, common video signal) for analog to digital conversion of the electronic pulses into converted pulses, a set of latches (FIG. 6 in view of FIG. 2, a series of

latches 57) wherein inputs of the latches are connected to outputs of respective comparators for recording passage of corresponding threshold voltages by rising edges of the converted pulses, a priority encoder (FIG. 6, enabling circuits 64) connected to outputs of the latches for determination of pulse height categories (FIG. 6, Bin 0, Bin 1, Bin 2, Bin 3, Bin 4, Bin 5, Bin 6 and Bin 7) consisting of converted pulses with a pulse height within pulse height intervals defined by the corresponding threshold voltages ((0v, 1.25v) for Bin 0, ((1.25v, 2.5v) for Bin 1, and so forth for bin 2, bin 3, bin 4, bin 5, bin 6 and finally bin 7, wherein the reference voltages progressively increase in steps of 1.25 volts), and a micro controller (FIGS. 1, 2 and 6, processor 19 includes a series of counters 58) that is adapted to count a number of pulses within each pulse of the height categories (From column 7, line 52 to column 8, line 27).

Kasdan et al. teaches all that is claimed as discussed above including the set of comparators (FIG. 6 in view of FIG. 2, a series of individual comparators 56), but it does not specifically teach the following feature:

- the threshold voltages of the comparators are non-equidistant from each other.

Flockencier teaches a system for processing reflected energy signals comprising:

With regard to claim 11, a set of comparators (FIG. 1, comparators 84) in which the threshold voltages of the comparators are non-equidistant from each other (spaced in logarithmic intervals) (Column 4, lines 15-28).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of configuring the comparators such that the threshold voltages of the comparators are spaced in logarithmic intervals (non-equidistant

from each other) taught by Flockencier since such an arrangement is beneficial to provide desirable and exemplary choices for a specific configuration of the comparators for processing data covering a large range of values, in which the logarithm scale is helpful to reduce the large range to a more manageable range.

With regard to claim 16, Kasdan et al. teaches that a plurality of sets of comparators (FIG. 6 in view of FIG. 2, a series of individual comparators 56) for pulse height determination of input electronic pulses of different amplification (FIG. 4, V_0, V_1, V_2, and so on).

With regard to claim 17, Kasdan et al. teaches that circuitry (FIG. 6 in view of FIG. 2, fixed frequency clock pulse generator 23) for resetting the latches (FIG. 6 in view of FIG. 2, a series of latches 57) a predetermined time period after start of a converted pulse, the time period being independent of the pulse height and pulse width (Column 8, lines 1-15).

7. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Koch et al. and Bee et al.

Kasdan et al. teaches all that is claimed as discussed in the above rejection of claims 11, 16 and 17 including pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- A filter for filtering the electronic pulses to provide filtered pulses having a substantially constant delay from pulse start to maximum pulse amplitude, and for providing the filtered pulses as the common input of the comparators.
- A filter for filtering the electronic pulses to provide an output signal containing filtered pulses with a DC-value substantially equal to zero.

Koch et al. teaches a fiber optic receiver comprising:

With regard to claim 13, a filter (Figure , DC blocking capacitor 58 and low pass filter 59) for filtering the electronic pulses to provide filtered pulses having a substantially constant delay and for providing the filtered pulses as an input of a comparator (Figure , comparator U2) (Column 4, lines 3-35).

With regard to claim 14, a filter (Figure , DC blocking capacitor 58 and low pass filter 59) for filtering the electronic pulses to provide an output signal containing filtered pulses with a DC-value substantially equal to zero (by using DC blocking capacitor 58) (Column 4, lines 3-35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of employing a filter for filtering the electronic pulses to provide a substantially constant delay and an output signal containing the filtered pulses with a DC-value substantially equal to zero taught by Koch et al. since Koch et al. teaches that such an arrangement is beneficial both to removes excess bandwidth from the amplitude limited pulsed voltage signal to reduce noise and to provide a constant group delay to minimize pulse overshoot and ringing as disclosed in column 4, lines 3-35, and to provide reduced ripple in the output with substantially constant delay through the filter to assure that the sync pulses do not exhibit time jitter with variations in amplitude, and to assure that the delay through the filter is substantially constant as disclosed in Bee et al., column 5, lines 32-38.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Iinuma.

Kasdan et al. teaches all that is claimed as discussed in the above rejection of claims 11, 12, 16 and 17 including pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- An integrated circuit comprising the pulse height analyzer.

Iinuma teaches a radiation imaging apparatus comprising:

With regard to claim 18, pulse-height analyzer sections 26 (FIG. 6) can be manufactured in an IC (integrated circuit) (Column 10, lines 17-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of manufacturing a pulse height analyzer using the recent semiconductor technology, for instance, Large Scale Integrated technology taught by Iinuma since Iinuma teaches that such an arrangement is beneficial to provide a circuit that is compact, highly reliable and which has a low cost as disclosed in column 10, lines 17-44.

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Miers.

Kasdan et al. teaches all that is claimed as discussed in the above rejection of claims 11, 12, 16 and 17 including the pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- A field programmable gate array comprising a pulse height analyzer.

Miers teaches an apparatus for filtering a laser beam in an analytical instrument comprising:

With regard to claim 19, a field programmable gate array (FIG. 14, FPGA 1308) comprising a pulse height analyzer (Column 43, lines 49-52).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of a field programmable gate array comprising a pulse height analyzer taught by Miers since such an arrangement is beneficial to provide desirable and exemplary choices for a specific configuration of the pulse height analyzer for a field programmable gate array.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Tumer et al.

Kasdan et al. teaches all that is claimed as discussed in the above rejection of claims 11, 12, 16 and 17 including the pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- An application specific integrated circuit comprising a pulse height analyzer.

Tumer et al. teaches an X-ray and gamma ray detector readout system comprising:

With regard to claim 20, an application specific integrated circuit (FIG. 1) comprising a pulse height analyzer (Paragraphs [0058] and [0125]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of an application specific integrated circuit comprising a pulse height analyzer taught by Tumer et al. since Tumer et al. teaches that such an arrangement is beneficial to provide a complete, highly integrated, low power readout ASIC

optimized for high resolution while minimizing system complexity and cost which are desirable and exemplary choices for a specific configuration of the pulse height analyzer for an ASIC as disclosed in paragraphs [0055], [0058] and [0125].

11. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Flockencier as applied to claim 11 above, and further in view of Koch et al. and Bee et al.

Kasdan et al. and Flockencier teach all that is claimed as discussed in the above rejection of claims 11, 16 and 17 including pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- A filter for filtering the electronic pulses to provide filtered pulses having a substantially constant delay from pulse start to maximum pulse amplitude, and for providing the filtered pulses as the common input of the comparators.
- A filter for filtering the electronic pulses to provide an output signal containing filtered pulses with a DC-value substantially equal to zero.

Koch et al. teaches a fiber optic receiver comprising:

With regard to claim 13, a filter (Figure , DC blocking capacitor 58 and low pass filter 59) for filtering the electronic pulses to provide filtered pulses having a substantially constant delay and for providing the filtered pulses as an input of a comparator (Figure , comparator U2) (Column 4, lines 3-35).

With regard to claim 14, a filter (Figure , DC blocking capacitor 58 and low pass filter 59) for filtering the electronic pulses to provide an output signal containing filtered pulses with a

DC-value substantially equal to zero (by using DC blocking capacitor 58) (Column 4, lines 3-35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of employing a filter for filtering the electronic pulses to provide a substantially constant delay and an output signal containing the filtered pulses with a DC-value substantially equal to zero taught by Koch et al. since Koch et al. teaches that such an arrangement is beneficial both to removes excess bandwidth from the amplitude limited pulsed voltage signal to reduce noise and to provide a constant group delay to minimize pulse overshoot and ringing as disclosed in column 4, lines 3-35, and to provide reduced ripple in the output with substantially constant delay through the filter to assure that the sync pulses do not exhibit time jitter with variations in amplitude, and to assure that the delay through the filter is substantially constant as disclosed in Bee et al., column 5, lines 32-38.

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Flockencier as applied to claim 1 above, and further in view of Iinuma.

Kasdan et al. and Flockencier teach all that is claimed as discussed in the above rejection of claims 11, 12, 16 and 17 including pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- An integrated circuit comprising the pulse height analyzer.

Iinuma teaches a radiation imaging apparatus comprising:

With regard to claim 18, pulse-height analyzer sections 26 (FIG. 6) can be manufactured in an IC (integrated circuit) (Column 10, lines 17-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of manufacturing a pulse height analyzer using the recent semiconductor technology, for instance, Large Scale Integrated technology taught by Iinuma since Iinuma teaches that such an arrangement is beneficial to provide a circuit that is compact, highly reliable and which has a low cost as disclosed in column 10, lines 17-44.

13. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Flockencier as applied to claim 11 above, and further in view of Miers.

Kasdan et al. and Flockencier teach all that is claimed as discussed in the above rejection of claims 11, 12, 16 and 17 including the pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- A field programmable gate array comprising a pulse height analyzer.

Miers teaches an apparatus for filtering a laser beam in an analytical instrument comprising:

With regard to claim 19, a field programmable gate array (FIG. 14, FPGA 1308) comprising a pulse height analyzer (Column 43, lines 49-52).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of a field programmable gate array comprising a pulse height analyzer taught by Miers since such an arrangement is beneficial to

provide desirable and exemplary choices for a specific configuration of the pulse height analyzer for a field programmable gate array.

14. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasdan et al. in view of Flockencier as applied to claim 11 above, and further in view of Tumer et al.

Kasdan et al. and Flockencier teach all that is claimed as discussed in the above rejection of claims 11, 12, 16 and 17 including the pulse height analyzer (FIG. 2, analysis system incorporated in the processor 19 of FIG. 1), but it does not specifically teach the following feature:

- An application specific integrated circuit comprising a pulse height analyzer.

Tumer et al. teaches an X-ray and gamma ray detector readout system comprising:

With regard to claim 20, an application specific integrated circuit (FIG. 1) comprising a pulse height analyzer (Paragraphs [0058] and [0125]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the diffraction pattern amplitude analysis for use in fabric inspection of Kasdan et al. to incorporate the teaching of an application specific integrated circuit comprising a pulse height analyzer taught by Tumer et al. since Tumer et al. teaches that such an arrangement is beneficial to provide a complete, highly integrated, low power readout ASIC optimized for high resolution while minimizing system complexity and cost which are desirable and exemplary choices for a specific configuration of the pulse height analyzer for an ASIC as disclosed in paragraphs [0055], [0058] and [0125].

Allowable Subject Matter

15. Claims 15 and 21-28 are allowed.

16. The following is an examiner's statement of reasons for allowance:

With regard to claim 15, applicants' arguments in the second paragraph at page 12 of 13 and amendments have been considered and found persuasive. Please see the previous Office Action mailed on August 1, 2008 for the examiner's statement of reasons for allowance.

With regard to claims 21-28, these claims are allowed at least by virtue of their dependency from the base claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

17. Applicant's arguments with respect to claims 11, 13, 14, 16-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAI-AN D. NGUYEN whose telephone number is (571)272-2170. The examiner can normally be reached on MON-THURS. (6:45 - 5:15).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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